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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/081,992	02/21/2002	Been-Yih Jin	10559-587001 / P12768	1734

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EXAMINER	
POMPEY, RON EVERETT	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 09/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/081,992	JIN ET AL.	
	Examiner	Art Unit	
	Ron E Pompey	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8 and 10-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8 and 10-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 8 and 10-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (US 5,545, 574) in further view of Yu (US 6,100,120) and Eguchi (US 5,185,286).

Chen discloses the limitations of:

a semiconductor substrate, the substrate being substantially free of silicon (20, fig. 2);

a gate dielectric layer (24, fig. 2) formed over a portion of the substrate; and

a gate electrode, source and drain regions (26, 32 and 34, fig. 4) further comprising (col. 2, ln. 54 – col. 3, ln. 14): an interlayer dielectric layer (92, fig. 9) over the gate, source and drain (col. 4, lns. 31-35). Chen does not explicitly describe that the well and source and drain are different type of dopants, however it is inherent and well know that if you have an n-type of transistor that the well and source and drain regions are of different type dopants. Chen does disclose that the device formed is an n-channel device (col. 5, ln. 2).

Chen discloses the limitations of the claimed invention except, wherein the gate dielectric comprises a material having a dielectric constant greater than about 10

wherein the thickness is large enough to prevent a portion of off-state leakage and the interlevel dielectric defines first, second and third openings in the interlayer dielectric layer and further comprising: a metal within the first, second and third openings in contact with gate electrode, source and drain regions.

However, Yu discloses the limitations of forming a gate dielectric with a dielectric constant greater than about 10 (col. 4, lns. 28-31; 22, fig. 4). Yu shows that it is well known in the art to use high dielectric constant materials for gate dielectrics therefore the physical thickness of the gate dielectric has less direct tunnel leakage.

Also, Eguchi discloses the limitations of forming contacts to the device (col. 4, lns. 30-36; 11, 12, 13 and 14, fig. 3). Therefore it would have been obvious to one of ordinary skill in the art to combine Eguchi with Chen, because the contacts allow for electrical communication to the MOS device from external devices.

Claim Rejections - 35 USC § 112

2. Claims 8 and 19 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The newly added claim matter: "a gate electrode defined over a portion of the gate dielectric laver such that the gate dielectric layer has a cross-sectional area substantially similar to a cross-sectional area of the gate electrode", is not described in the specification.

Response to Arguments

3. Applicant's arguments filed 8-20-04, pertaining to claims 8 and 10-21, have been fully considered but they are not persuasive. The applicant argues that the prior art of record fails to disclose: "a gate electrode defined over a portion of the gate dielectric laver such that the gate dielectric layer has a cross-sectional area substantially similar to a cross-sectional area of the gate electrode". However, since the gate and dielectric are patterned to the same dimensions, in the prior art reference(s), the cross-sectional area will be substantially similar.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ron E Pompey whose telephone number is (571) 272-1680. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Ron Pompey
AU: 2812
September 20, 2004

John F. Niebling
Supervisory Patent Examiner
Technology Center 2800